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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/747,118 | 12/22/2000 | Benjamin N. Eldridge | P3D5-US | 3104 |

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| EXAMINER |
|---|
| ALCALA, JOSE H |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/747,118 | ELDRIDGE ET AL. | |
| | Examiner | Art Unit | |
| | Jose H Alcala | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 March 2003* .

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *60-66,68 and 347-361* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *60-68,347-349 and 351-361* is/are rejected.

7)☒ Claim(s) *350* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

## DETAILED ACTION

1. This non-final final rejection is in response to amendment filed on 3/24/03.

### *Response to Arguments*

2. Applicant's arguments with respect to claims 60-66, 68, 347-361 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 60-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Burdick (US Patent No. 5,255,431).

Regarding Claim 60, Burdick teaches an electronic assembly (Device of figure 1), comprising: a first plurality of semiconductor dies (reference number 60) mounted edge-to-edge, in close proximity to one another, on a first side of a printed circuit board (reference number 44), each semiconductor die electrically connected to the printed circuit board by free-standing, resilient contact structures (reference number 66) mounted to each of the semiconductor dies.

Regarding Claim 61, the recitation: " that the semiconductor dies are memory devices" is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding Claim 62, the recitation: " the electronic assembly is a single in-line memory module (SIMM)" is just a mere label for the device claimed, suggesting an intended use for the device.

Regarding Claim 63, Burdick teaches that the resilient contact structures are compliant.

Regarding Claim 64, Burdick teaches further comprising a second plurality of semiconductor dies (reference numbers 32 and 34) mounted to a second side of the printed circuit board. See figure 1.

5. Claims 347-349 are rejected under 35 U.S.C. 102(e) as being anticipated by Pai et al. (US Patent No. 5,317,479).

Regarding Claim 347, Pai teaches a semiconductor package (Device of Figure 5B) comprising: first insulating layer (reference number 54); first conductive layer (reference number 57) disposed on a first surface of the first insulating layer and patterned to have a first plurality of conductive traces; second insulating layer (reference number 90); second conductive layer (reference number 55) disposed on a first surface of the second insulating layer and patterned to have a second plurality of conductive

traces; the first conductive layer being in contact with the second insulating layer (through reference number 50); the second conductive and insulating layers are arranged and disposed so that outer portions of the first plurality of conductive traces are exposed (See Figure 5B); a first plurality of electrical contact structures (reference number 50) mounted to outer portions of the first plurality of conductive traces; and a second plurality of electrical contact structures (electrical contact attaching reference number 94 and 92, to reference number 90) mounted to the second plurality of conductive traces. (See Figure 5B)

Regarding Claim 348, Pai teaches that the first plurality of electrical contact structures extends to a plane (the plane at the bottom surface of reference number 90); and the second plurality of electrical contact structures extend to the plane (the plane at the bottom surface of reference number 90). (See Figure 5B)

Regarding Claim 349, Pai inherently teaches that the first plurality of electrical contact structures are resilient contact structures; and the second plurality of electrical contact structures are resilient contact structures.

6. Claims 358-361 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (US Patent No. 4,667,219).

Regarding Claim 358, Lee teaches a semiconductor die (Reference number 18) having a front surface (top surface) and a back surface (bottom surface); and a plurality of free-standing resilient contact structures (Reference number 84) mounted to the front surface of the semiconductor die.

Regarding Claim 359, Lee teaches a semiconductor device (Reference number 18), further comprising: conductive pads (reference number 86) disposed on the front surface of the semiconductor die; and wherein: one contact structure is mounted to each conductive pad. See Figure 8.

Regarding Claim 360, Lee teaches that the resilient contact structures each comprise: a wire stem, bonded at one end to the front surface of the semiconductor die and configured to have a springable shape; and an overcoat material applied over the wire stem and over a portion of the front surface of the semiconductor die. See Figure 9.

Regarding Claim 361, Lee teaches that the resilient contact structures are compliant.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 65,66,68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burdick (US Patent No. 5,255,431) in view of Lee et al. (US Patent No. 4,667,219).

Regarding Claim 65, Burdick teaches all the limitations of the instant claimed invention as stated supra for claim 60, but fails to explicitly teach that the freestanding resilient contact structures comprise: wires bonded to the semiconductor dies; and an overcoat covering at least a portion of the wires. Lee teaches a semiconductor element

connected to a circuit board, through freestanding resilient contact structures comprising: wires (reference number 84) bonded to the semiconductor dies; and an overcoat (See figure 9) covering at least a portion of the wires. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Burdick and Lee in order to have freestanding resilient contact structures comprising wires bonded to the semiconductor dies; and an overcoat covering at least a portion of the wires, thus accommodating any thermal expansion mismatch between the semiconductor device(s) and the circuit board, and reducing any strain that could be caused due to the manufacturing or assembling procedures.

Regarding Claim 66, Burdick as modified by Lee, teaches that the freestanding resilient contact structures comprise plated wires adhered to the semiconductor dies (See figure 9).

Regarding Claim 68, Burdick as modified by Lee, teaches a rigidizing material encapsulating at least a portion of the resilient contact structure (See figure 9).

9. Claim 351-357 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Patent No. 4,667,219) in view of Nelson et al. (US Patent No. 5,265,321).

Regarding Claim 351, Lee teaches a semiconductor device (Figure 8), comprising: a semiconductor die (reference number 18) having a front surface (top surface) and a back (bottom surface) surface; a plurality of free-standing interconnect structures (References number 84) mounted to the front surface of the semiconductor die; and a free-standing heat dissipating structure (References number 16) mounted to the back surface of the semiconductor die. Lee fails to explicitly teach that instead of

having one free-standing heat dissipating structure, there is a plurality of free-standing heat dissipating structures. Nelson teaches a semiconductor device having a plurality of free-standing heat dissipating structures (reference number 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lee and Nelson in order to have a plurality of free-standing heat dissipating structures, thus providing a more reliable, lower thermal resistance combination due to thinner bond line attachment.

Regarding Claim 352, Lee teaches that the interconnect structures are resilient contact structures.

Regarding Claim 353, Lee teaches that the interconnect structures are compliant contact structures.

Regarding Claim 354, Lee as modified by Nelson teaches that free-standing heat-dissipating structures are wires mounted to the back surface of the semiconductor die.

Regarding Claim 355, Lee as modified by Nelson teaches that the free-standing interconnect structures are of a first material (cooper); and the free-standing heat-dissipating structures are of a second material (aluminum) which is different from the first material.

Regarding Claim 356, Lee as modified by Nelson fail to explicitly teach that: "the free-standing interconnect structures and the free standing heat-dissipating structures are overcoated with a common material. It would have been obvious to overcoat the free standing heat-dissipating structures with the same material as the free-standing

interconnect structures, in order to further increase the thermal conduction properties of the free standing heat-dissipating structures.

Regarding Claim 357, Lee as modified by Nelson teaches: "a layer of a metallic material (reference 22 of Nelson) disposed between the free standing heat-dissipating structures and the back surface oft the semiconductor die, the interconnect structures are resilient contact structures.

***Allowable Subject Matter***

10. Claim 350 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

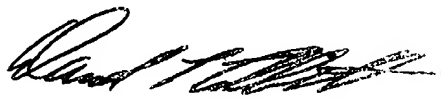
The prior art fails to teach, disclose, or suggest, either alone or in combination, at least on claim 350, a semiconductor package comprising: the second conductive and insulating layers are arranged and disposed so that inner portions of the first plurality of conductive traces are exposed for connecting to a semiconductor device; and further comprising means for connecting the semiconductor device to the exposed inner portions of the first plurality of conductive traces; and means for connecting the semiconductor device to the second plurality of conductive traces.

***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



JHA
June 16, 2003

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